ABSTRACT OF THE DISCLOSURE

Bit lines are arranged with minimum width and minimum space in a chip, and each bit line is given a maximum of first potential difference. The minimum space is the value which will not make a line short-circuit in a line due to dielectric strength, when the first potential difference is applied across the bit lines. This value may be the design rule or the minimum dimensions capable of being processed by lithography. A second potential difference lager than the first potential difference is applied across a shielded power line and the bit lines. The shielded power line is not adjacent to the bit lines in the wiring width direction in the area where the bit lines are arranged with the minimum space.